REV	Description	DATE	BY
A4A	Initial production Release.	11/19/2012	GC
A5	On the initial production release the processors were to be found incorrect as supplied by TI. Parts while marked AM3359 were actually AM3352. This revision uses the correct parts.	1/2/2013	GC
A5A	1. Deleted R29-R44 from the LCD lines. 2. Added 47pf capacitors C156-C173 to LCD data lines to ground. 3. Changed schematic revision to A5A. 4. Changed a few footprints after PCB update for above changes. 5. Added access point for the battery function of the TPS65217C. 6. Added Ferrite beads in series with LED power and 5V power rail of the USB host connector. Required to pass FCC/CE testing due to noise emissions on that pin. 7. Added power button to enable sleep, wakeup, power down and power up features on the system. 8. Added Modification to add 100K ohm resistor to ground to prvent crosstalk when serial cable is not plugged in.	2/8/2013	GC
A5B	1. Added 100K pulldown on J1 pin 4 to prevent crosstalk when serial cable is not connected into PCB layout. 2. Changed the LED resistors to 4.75K to lower the brightness.	5/21/2013	GC
A5C	1. Changed R46, R47,R48 to 0 ohms. 2. Changed R45 to 22 Ohms. Change was made due to production failures on some boards due to differences in impedances.	6/12/2013	GC
A6	1. Moved the enable for the VDD_3V3B regulator to VDD_3V3A rail. Change was made to reduce the delay between the ramp up of the 3.3V rails. 2. Added a AND gate to the SYS_RESETn circuitry. There is a small chance that on power up the nRESETOUT signal on the processor may go high, causing the SYS_RESETn signal to go HI before it should. This change reenforces the reset with the PORZn reset signal. 3. Added optional zero ohm resistor to tie GND_OSC0 to system ground.	7/25/2013	GC
A6A	1. Added optional zero ohm resistor to tie GND_OSC1 to system ground. 2. Changed C106 to a 1uF capacitor. 3. Changed C24 to a 2.2uF capacitor. 4. Made R8 installed and R9 not installed.	12/13/2013	GC
B	1.Changed the processor to the AM3358BZCZ100.	1/20/2014	GC
C	1.Increased the eMMC from 2GB to 4GB.	3/21/2014	GC

PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	POWER MANAGEMENT
3	PROCESSOR 1 OF 3, JTAG HEADER
4	PROCESSOR 2 OF 3, UAB PORTS
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	DDR3 MEMORY
8	eMMC FLASH
9	10/100 ETHERNET
10	HDMI FRAMER
11	EXP CONN, uSD

NOTE: PCB Revision for this board is Rev B6

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Title: BeagleBone Black Cover Page		
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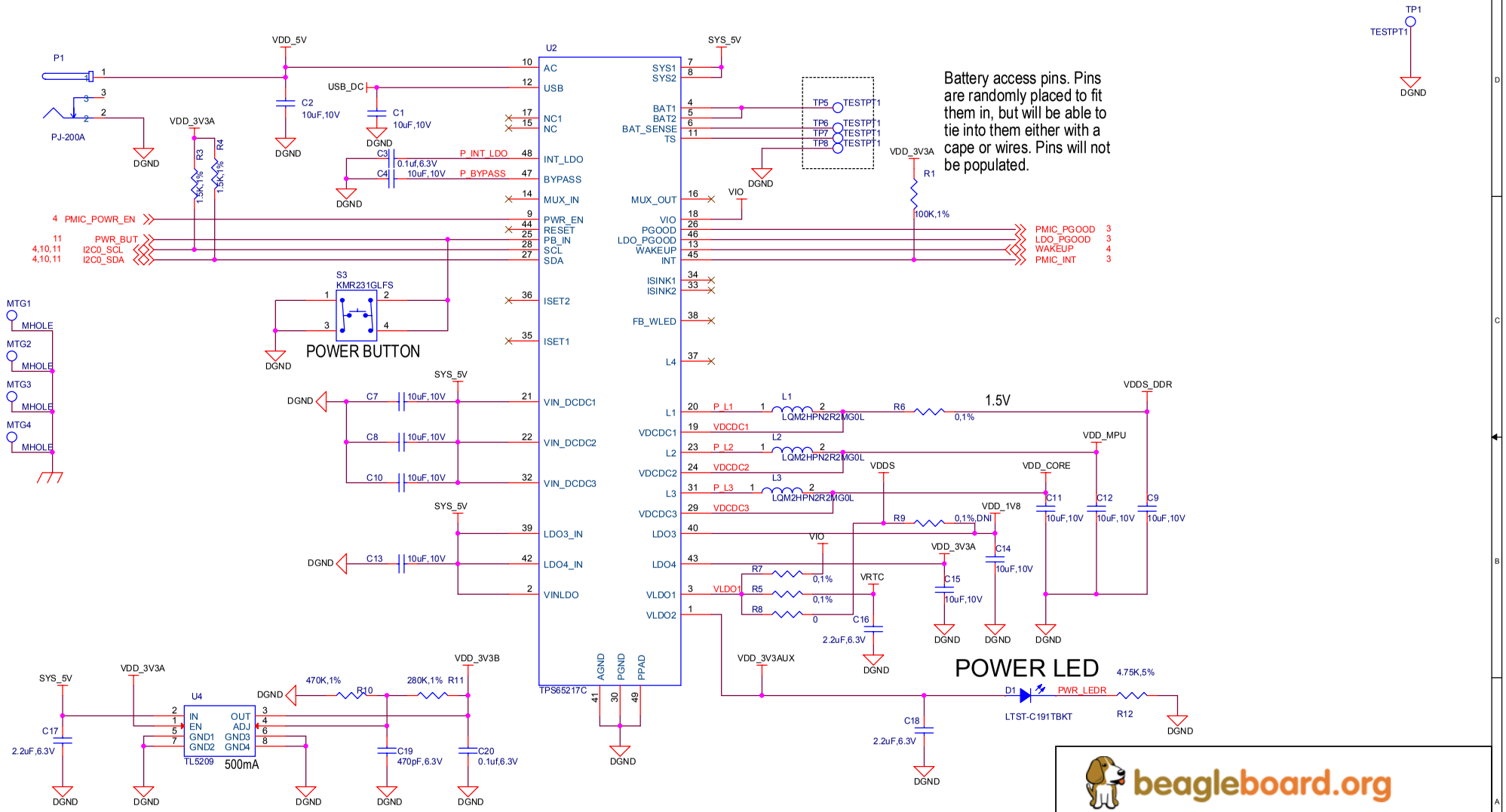

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Title	BeagleBone Black Power Management	
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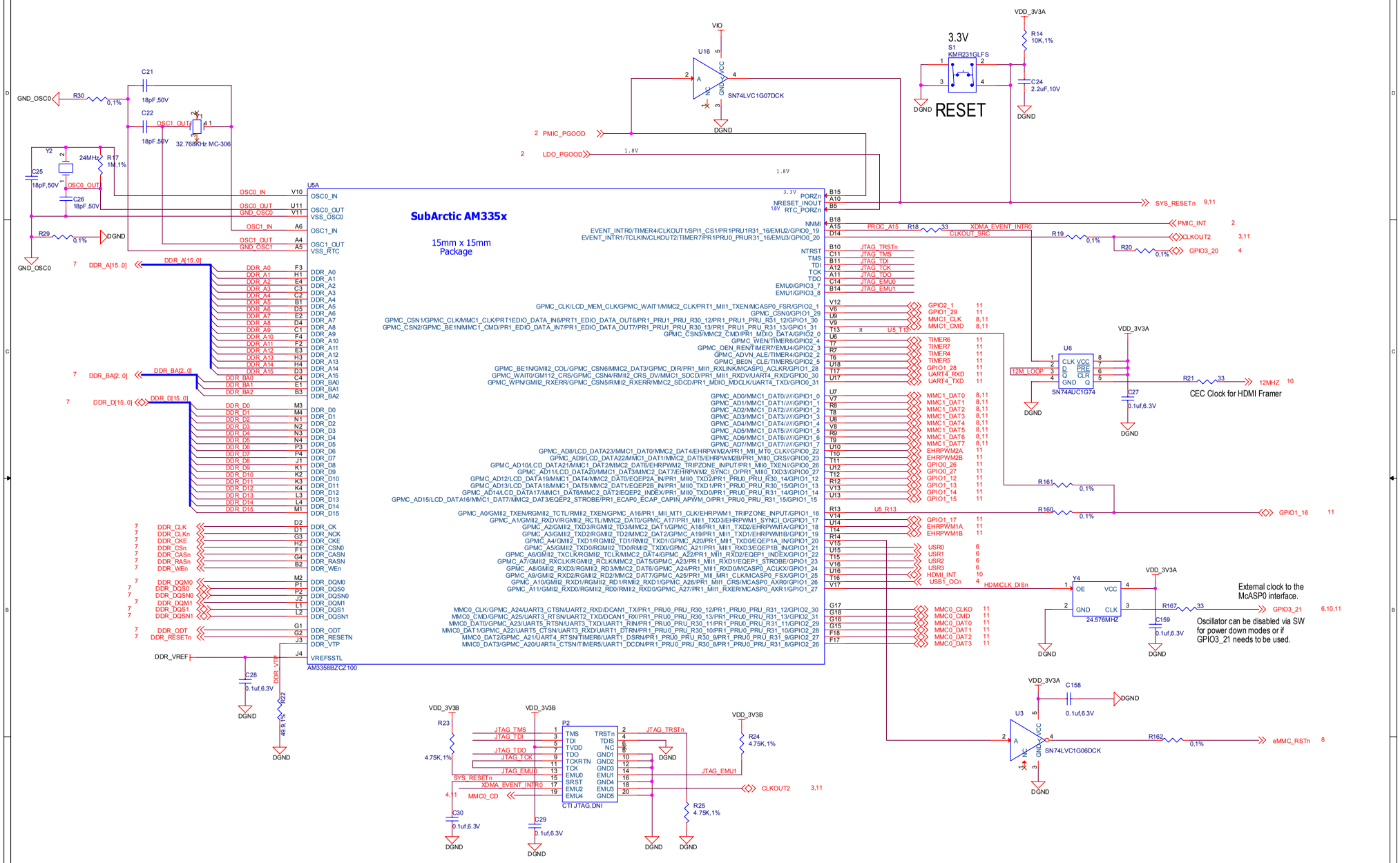

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Size: C	Document Number: 450-5500-001	Rev: C
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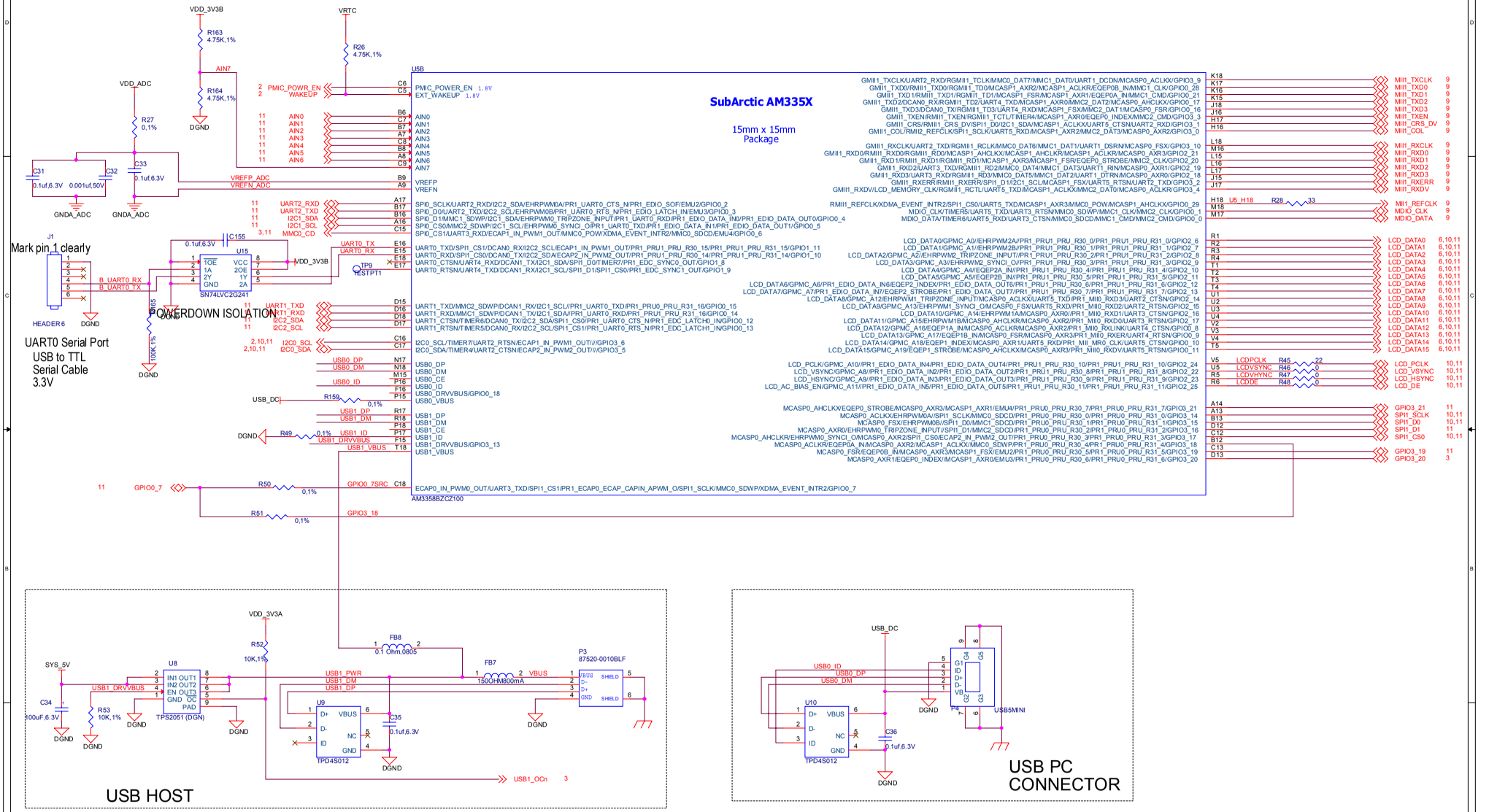

Title	BeagleBone Black Processor 2 of 3, USB, and Serial
Size	C
Document Number	450-5500-001
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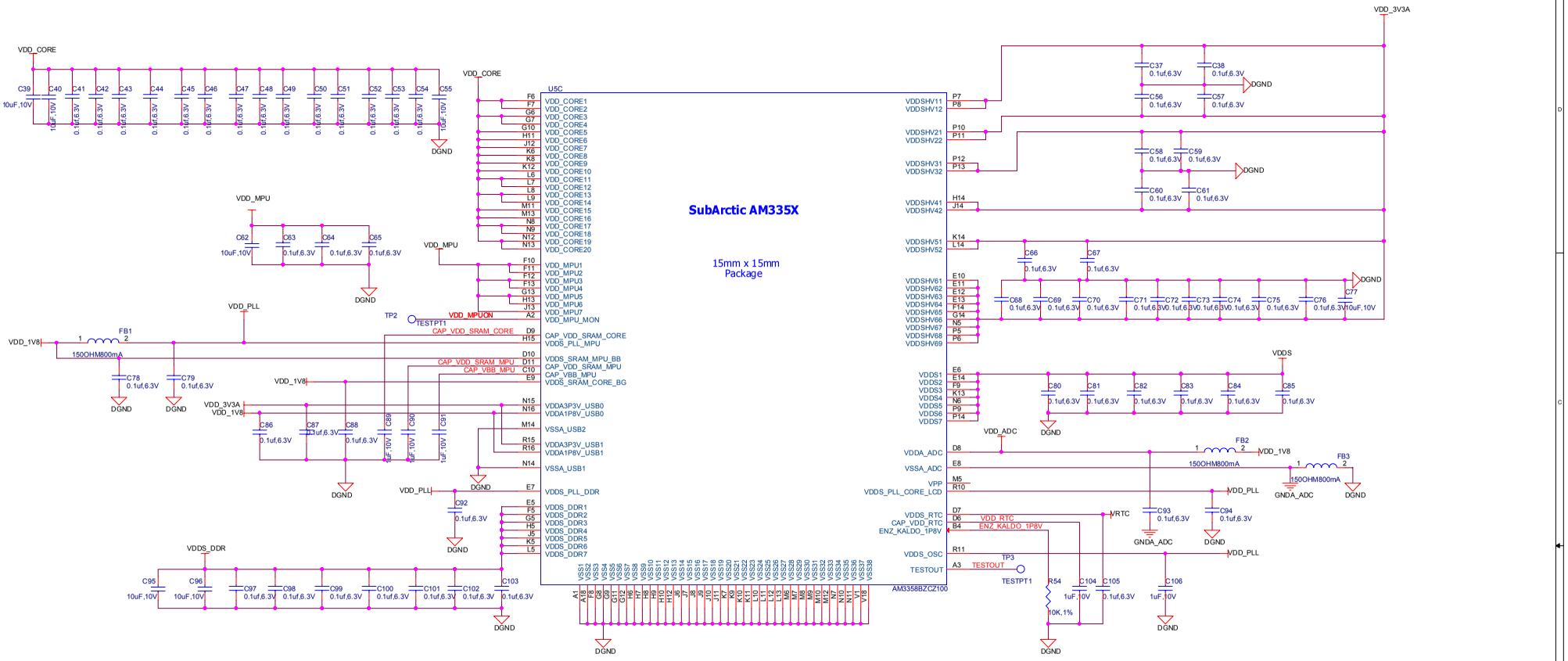

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Size: C	Document Number: 450-5500-001	Rev: C
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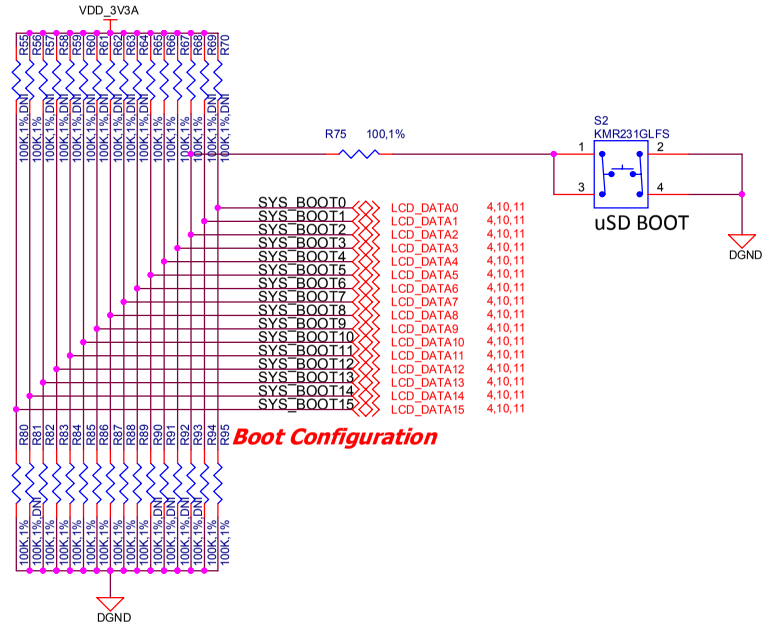

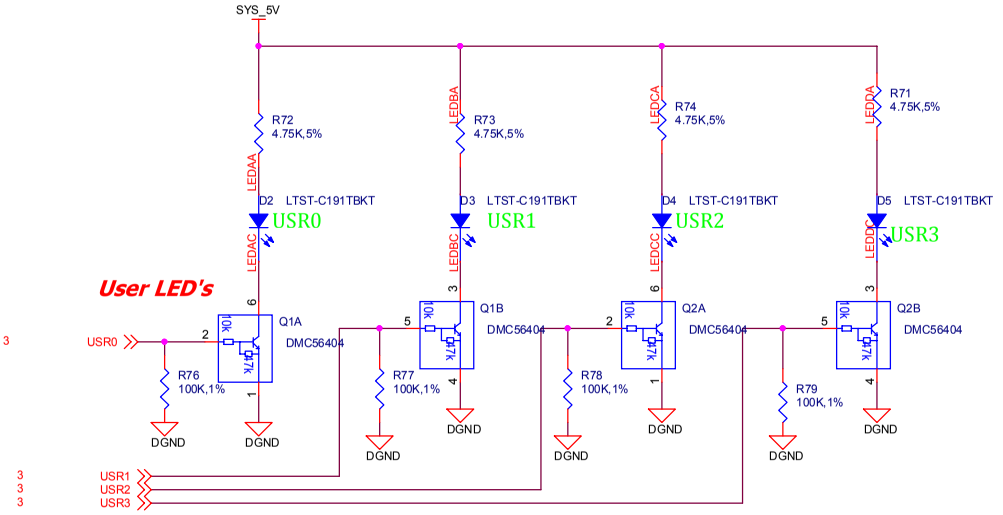

SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC1	MMC0	UART0	USB0[5]
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0	MMC0	USB0[5]	UART0

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Title	BeagleBone Black LED, Configuration, and Reset	
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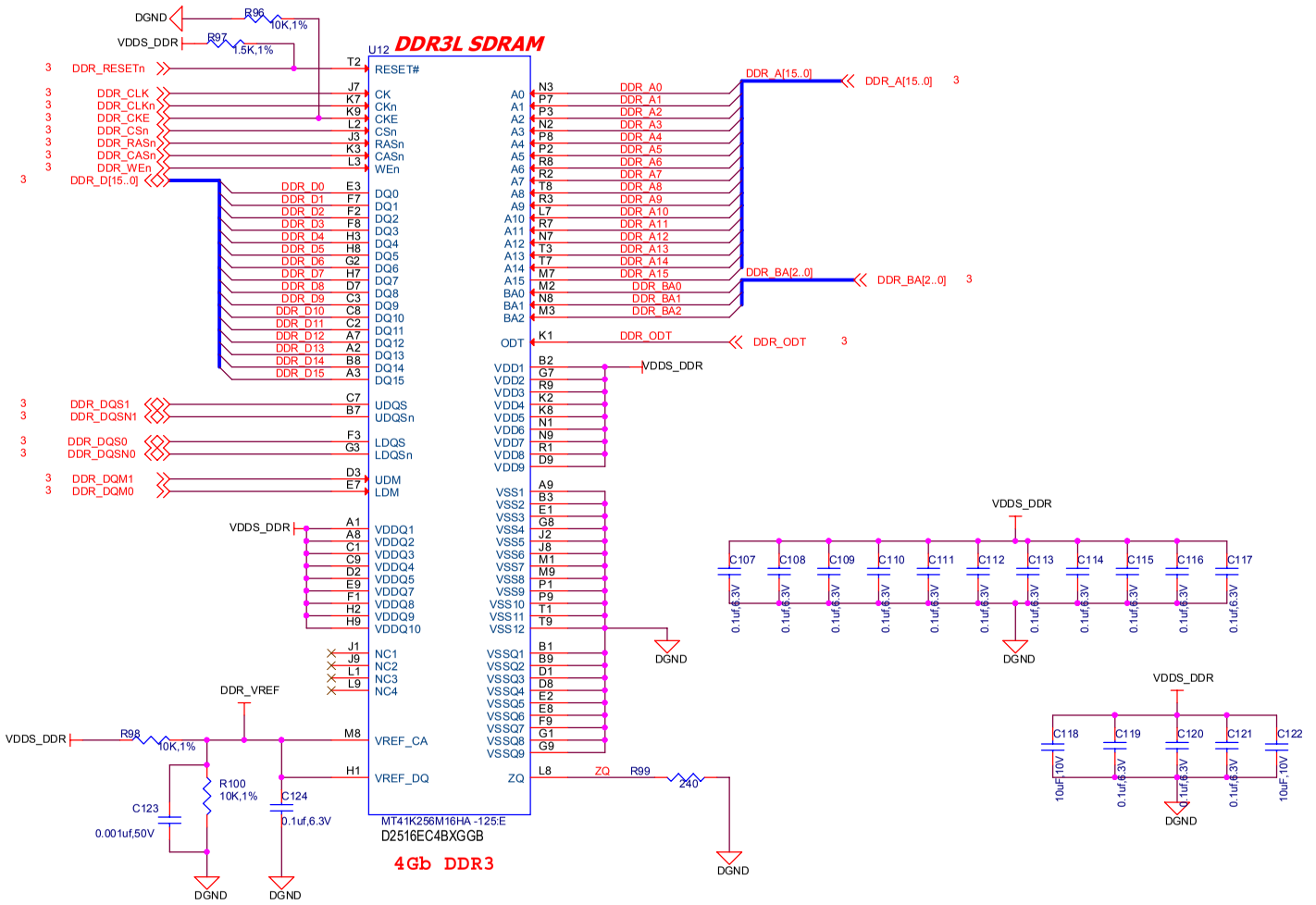

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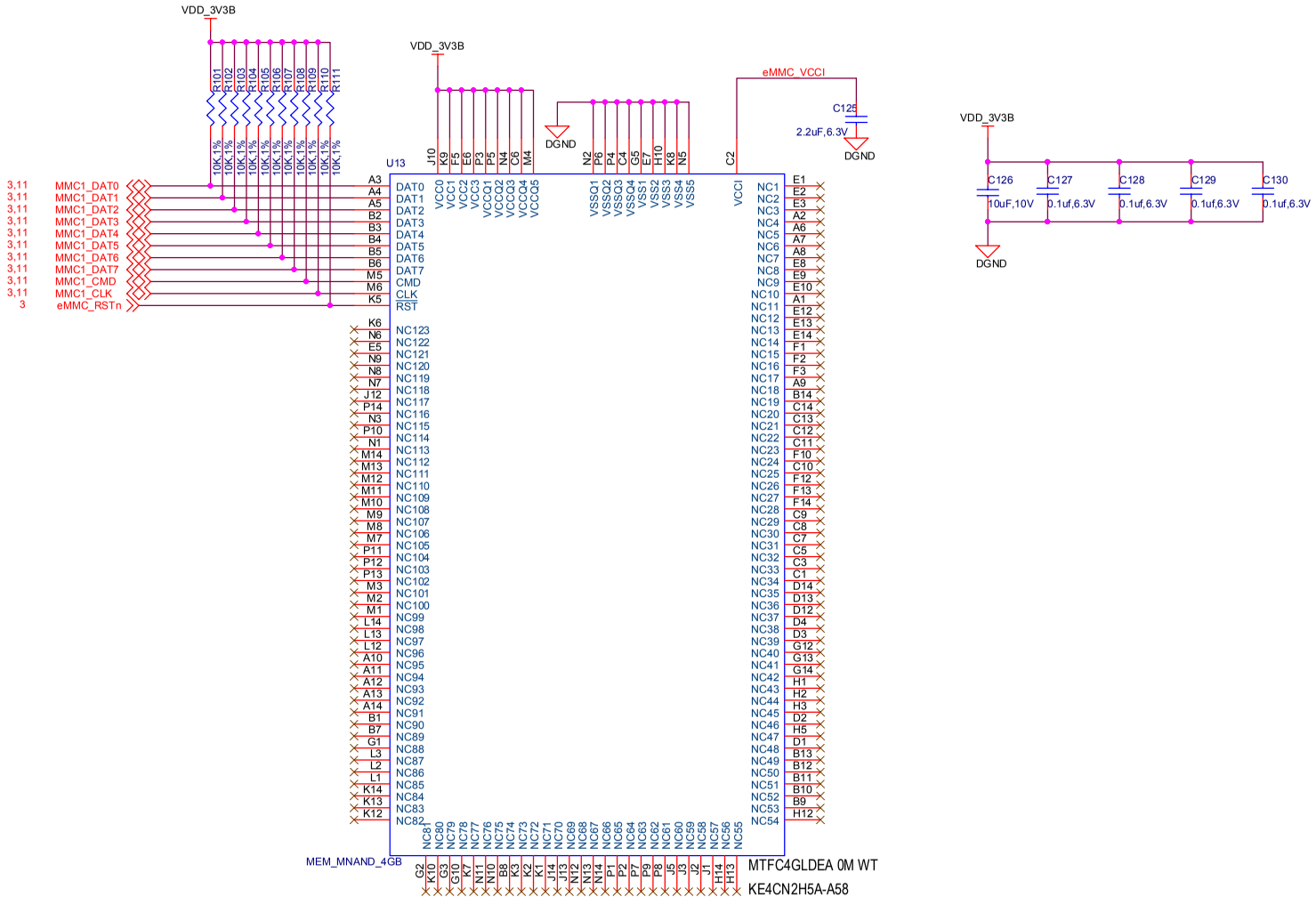
Title	BeagleBone Black DDR3 Memory	
Size: B	Document Number: 450-5500-001	Rev: C
Date: Wednesday, April 09, 2014	Sheet 7 of 11	



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Title	Beagle BoneBlack 4G eMMC	
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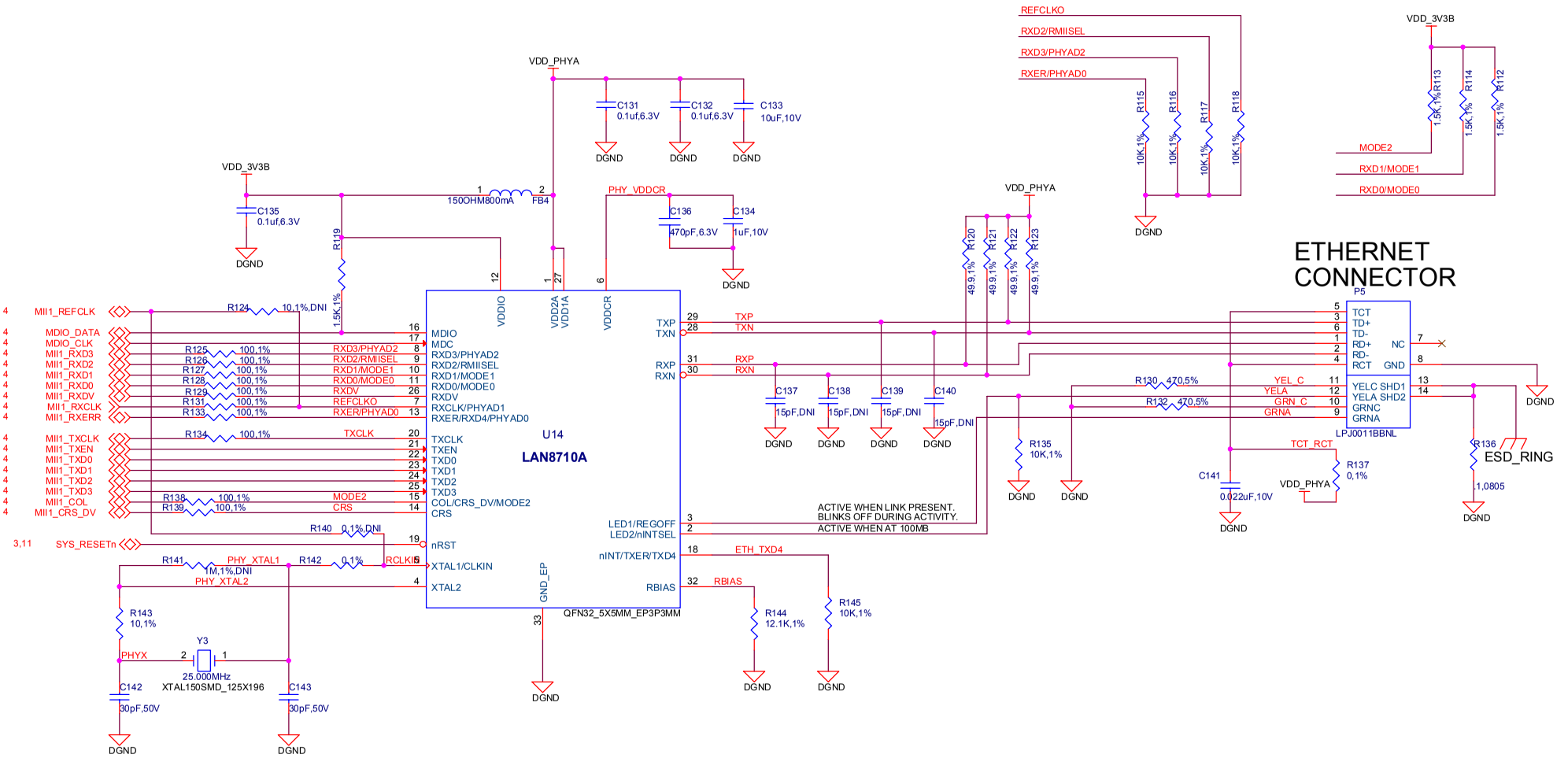

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Title	BeagleBone Black Ethernet	
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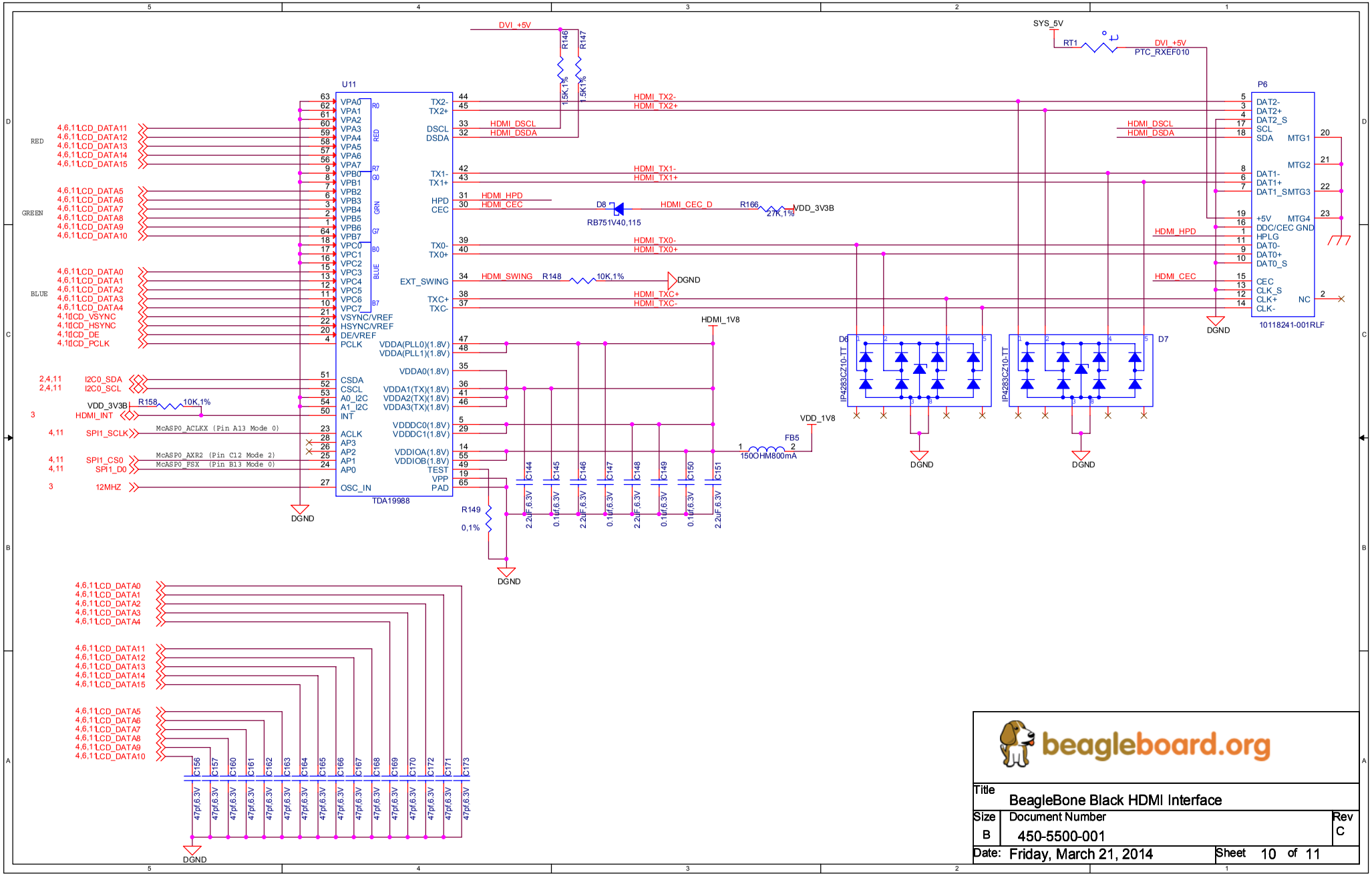

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Title	BeagleBone Black HDMI Interface	
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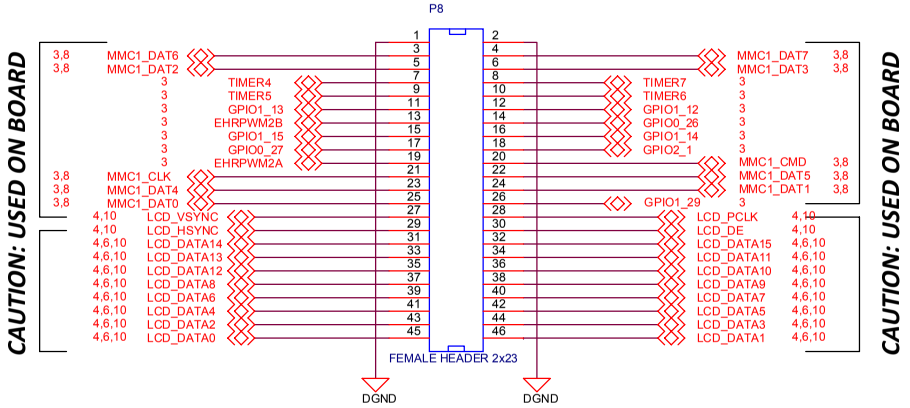
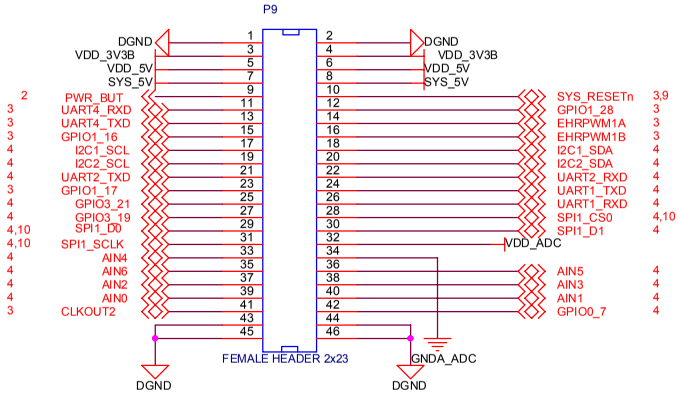


EXPANSION HEADER



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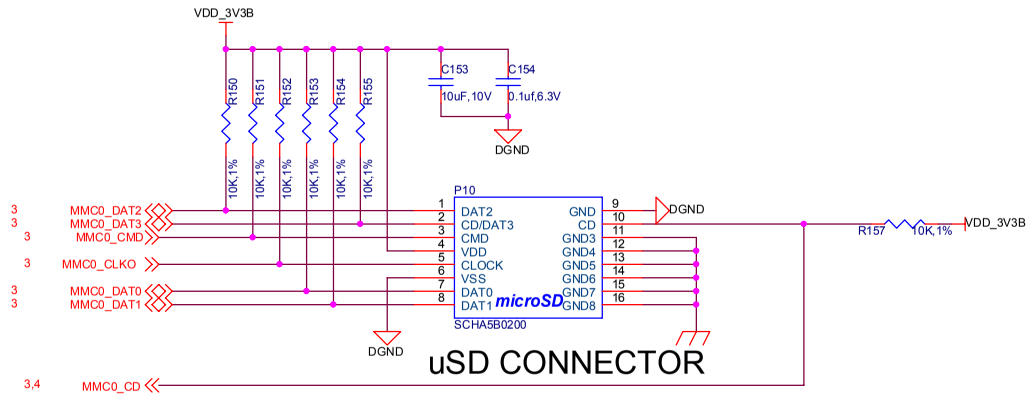

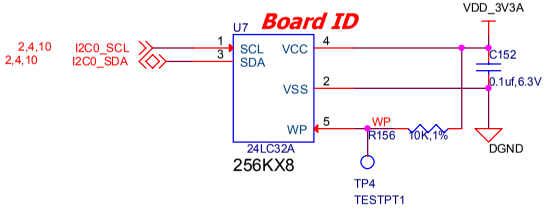

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Title	BeagleBone Black Expansion Headers, uSD.and EEPROM	
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