PCE243 OPT Evaluation Board
User Guide

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Revision History

Version	Release Date	Note
1.0	April 2003	First release

Note: This document is subject to change without notice.

Contents

1.0 OTG243: USB Host/Function/OTG Controller

1.1 Overview

TransDimension's OTG243 (TDI part number: TDOTG243-000C for 100 pin LQFP, and TDOTG243-00BC for 84 pin TF-BGA) is designed specifically for embedded applications. It is USB Specification 2.0 compliant, operating at full speed (12Mb/s) and/or low speed (1.5Mb/s). The controller supports all four types of USB transfers: Control, Interrupt, Bulk, and Isochronous with the high data throughput, and low interrupt rates. The transfer level programming makes the OTG243 very easy to use, ensuring rapid software development, and all levels of software are available from TransDimension and SoftConnex to support it. The block diagram of the OTG243 is shown in Figure 1. The OTG243 pin assignment is given in Figure 2.

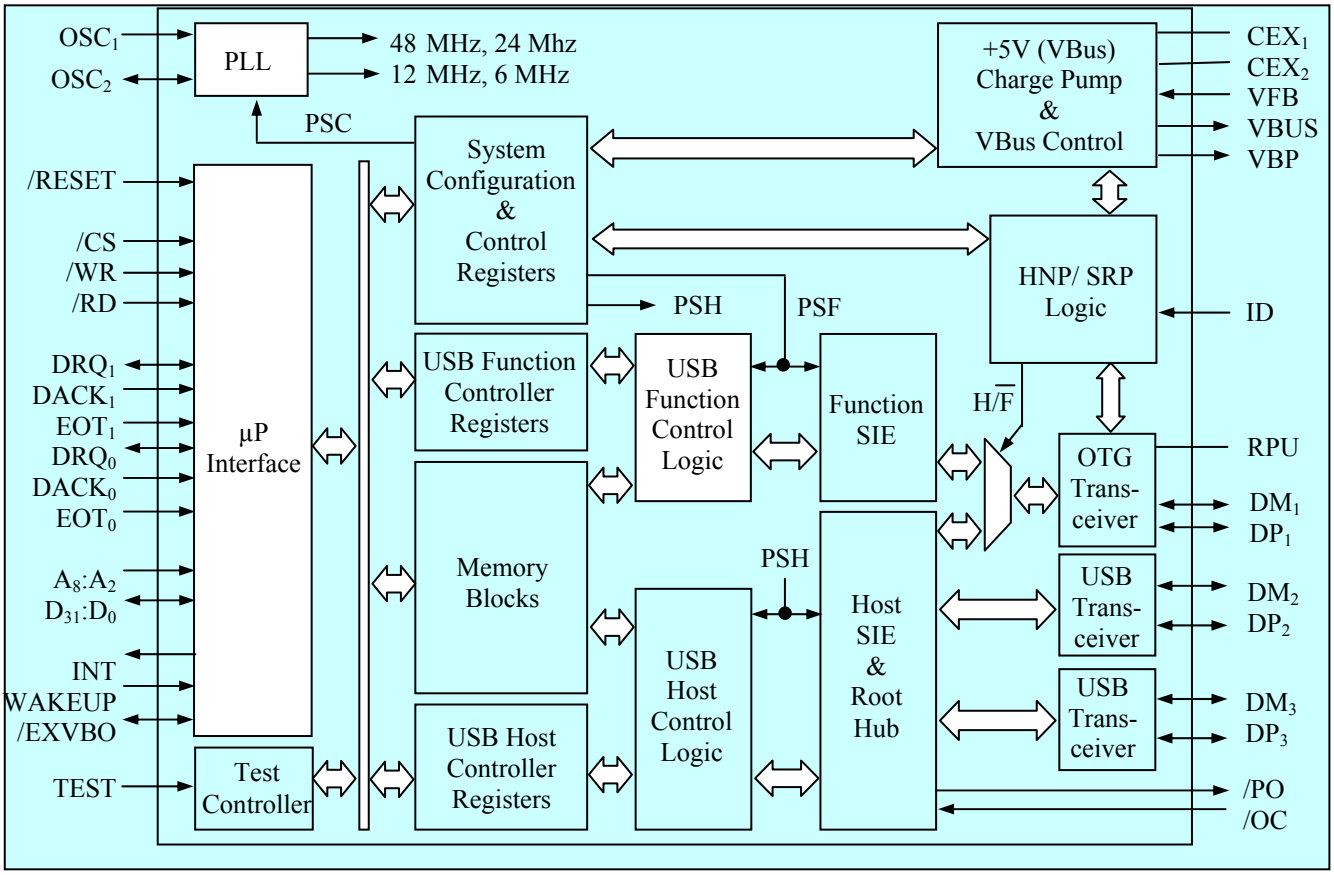


Figure 1: OTG243 Host/Function/OTG Controller

The OTG243 is ideal for low power embedded applications, including cell phones, palm platforms, PDAs, STBs, home gateway systems, and Internet appliances. Peer-to-Peer communication is made simple with the OTG243 as USB connectivity is achieved without PC intervention.

1	NC	21	V_{DD}	41	D_{26}	61	V_{DD}	81	VBUS
2	D_0	22	V_{DD}	42	D_{27}	62	V_{DD}	82	VFB
3	D_1	23	V_{SS}	43	V_{SS}	63	WAKEUP	83	/OC
4	D_2	24	TEST	44	V_{DD}	64	INT	84	/PO
5	V_{DD}	25	NC	45	DP_2	65	/RESET	85	ID
6	V_{DD}	26	/CS	46	DM_2	66	VBP	86	V_{SS}
7	D_3	27	/WR	47	DP_3	67	A_2	87	V_{DD}
8	D_4	28	/RD	48	DM_3	68	A_3	88	V_{DD}
9	D_5	29	D_{16}	49	NC	69	A_4	89	/EXVBO
10	D_6	30	D_{17}	50	NC	70	A_5	90	DRQ_1
11	D_7	31	D_{18}	51	NC	71	A_6	91	DRQ_0
12	V_{SS}	32	D_{19}	52	RPU	72	A_7	92	$DACK_1$
13	D_8	33	D_{20}	53	DP_1	73	A_8	93	$DACK_0$
14	D_9	34	D_{21}	54	DM_1	74	NC	94	EOT_1
15	D_{10}	35	D_{22}	55	V_{SS}	75	NC	95	EOT_0
16	D_{11}	36	D_{23}	56	D_{28}	76	AV_{DD}	96	V_{SS}
17	D_{12}	37	V_{DD}	57	D_{29}	77	AV_{SS}	97	AV_{SS}
18	D_{13}	38	V_{SS}	58	D_{30}	78	CEX_1	98	OSC_1
19	D_{14}	39	D_{24}	59	D_{31}	79	V_{DD}	99	OSC_2
20	D_{15}	40	D_{25}	60	V_{SS}	80	CEX_2	100	AV_{DD}

Figure 2: OTG243 pin assignment (100-pin LQFP)

1.2 OTG243 Operating Modes

The OTG243 chip can be configured by software to operate in several modes as described in Figure 3.

Mode	Port 1	Port 2	Port 3	Application
OTG/Host	OTG	Host	Host	OTG Dual Role Device (DRD) and USB host of two ports
Function/Host	Function	Host	Host	USB function and USB host of two ports
Host Only	Host	Host	Host	USB host of three ports

Figure 3: OTG243 Operating modes

1.3 Software Support

TransDimension, together with SoftConnex Inc, a wholly owned subsidiary, offers total solutions including controller chips, reference designs and developer kits, firmware for microprocessor interfacing, HCD (Host Controller Driver), HNP (Host Negotiation Protocol), SRP (Session Request Protocol) as well as USB host and function stacks running under most real time operating systems.

2.0 PCE243 OPT Evaluation Board Introduction

2.1 Usage

The PCE243 OPT (TDI part number TDOTG243-1190) is an evaluation/development board for the OTG243 chip. Measured at 3.5" by 5.5", it can be employed to:

- evaluate TransDimension's OTG243 USB Host/Function/OTG Controller;
- run OTG243 demonstrations;
- develop user software for OTG243 based applications; and
- serve as a subassembly in an OEM's product to provide USB host/function/OTG support.

Note that while the PCE243 OPT can be used to evaluate the OTG243, it will not result in optimal performance, due to the long cycle times of the PCI bus. For optimal performance evaluation, the OTG243 should be placed directly on the system bus.

2.2 PCE243 OPT Chip Placement Diagram

The PCE243 OPT is a PCI add-in card for USB On-the-Go development, utilizing the Transdimension OTG243. Figure 2-1 illustrates the chip placement diagram for the PCE243 OPT development board. The board is comprised of the PLX 9030, Farchild Semiconductor 93CS66, Lattice isp2064, Texas Instruments TPS2044, and the Transdimension OTG243.

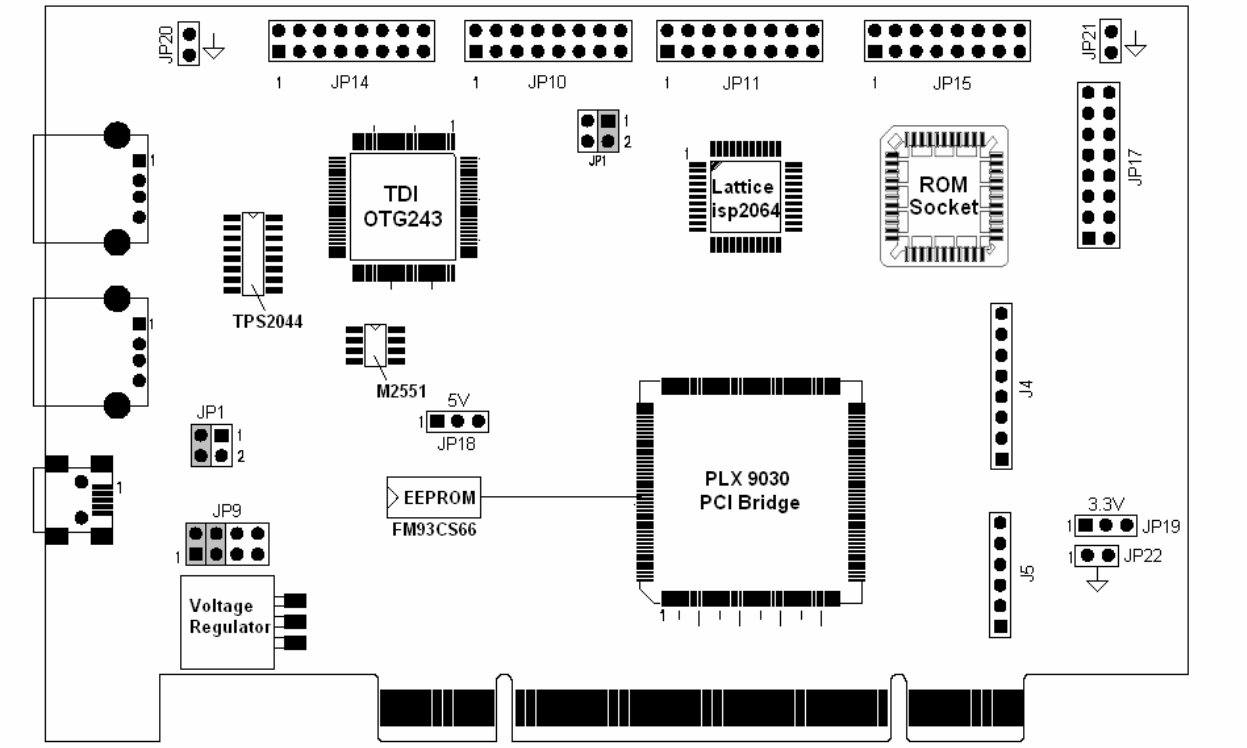


Figure 2-1. PCE243 OPT PCI add-in card Diagram

PLX 9030

The PLX 9030 is a 32-bit, 33-MHz PCI Bus general-purpose PCI Target device. It acts as a PCI bridge for the OTG243. The PLX 9030 handles all of the PCI signaling and software interfacing and translates the PCI bus cycles to a simple control, address, data general interface for easy connectivity of memory and I/O devices, such as the OTG243.

Lattice isp2064

The ispLSI 2064 is a High Density Programmable Logic Devices. The devices contain 64 Registers, 64 Universal I/O pins, four Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The IspLSI2064 is used to control a number of options on the board, and is capable of generating interrupts when specific events occur.

Fairchild 93C66

FM93CS66 is a 4096-bit CMOS non-volatile EEPROM organized as 256 x 16-bit array. This device features MICROWIRE interface which is a 4-wire serial bus with chipselect (CS), clock (SK), data input (DI) and data output (DO) signals. The FM93C66 is used to store the “boot-up” configuration for the PLX9030. That is, the PCI configuration register space information is stored within the FM93C66 and when the unit is initially powered on; the PLX9030 loads the information from the FM93C66.

Texas Instruments TPS2044

The TPS2044 and TPS2054 quad power distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. On the PC243, the TPS2044 is used to control power to the USB ports and is controlled by the OTG243.

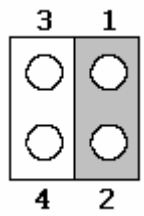
ROM Socket

The PCE243 OPT contains a ROM socket for future expansion. The ROM socket can provide a boot expansion ROM such that, as the computer system is initialized, the ROM bios will read and execute code from the expansion ROM.

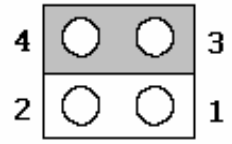
3.0 Jumpers and Headers

3.1 JP1 – VBUS Power

Jumpers 1-2 and 3-4 are mutually exclusive jumpers. If jumpers 1-2 are closed, then jumpers 3-4 should be open. Conversely, if jumpers 3-4 are closed, then jumpers 1-2 should be open.

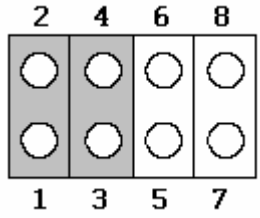
JP1	Pins	Description
	1-2	Closed: Internal Bus power Open:
	3-4	Closed: External Bus power Open:

3.2 JP16 – OTG243 Mode

JP16	Pins	Description
	1-2	Closed: 16 bit Operation Open: 32 bit Operation Default: Open
	3-4	Closed: Normal Operation Open: Test Mode Default: Closed

3.3 JP9 – PCI Power

Jumpers 1-2, 3-4 are mutually exclusive jumpers from pairs 5-6, 7-8. If jumpers 1-2, 3-4 are closed, then jumpers 5-6, 7-8 should be open. Conversely, if jumpers 5-6, 7-8 are closed, then jumpers 1-2, 3-4 should be open.

JP9	Pins	Description
	1-2	Regulated 5V to 3.3V from PCI Bus
	3-4	Regulated 5V to 3.3V from PCI Bus
	5-6	3.3V from PCI Bus
	7-8	3.3V from PCI Bus

4.0 PCI Operation

4.1 PCE243 OPT Device Discovery

Every PCI function must implement a PCI configuration space, where the PCI configuration registers are found. PCI Configuration registers are accessed with read and write operations to the PCI configuration space, which is separate from Memory and I/O space. Table 4-1 lists the standard PCI configuration register space for all PCI functions on the PCI bus.

Table 4-1. Standard PCI Configuration Register Space.

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID		Vendor ID		00h
Status Register		Command Register		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
Base Address Register 0 (BAR 0)				10h
Base Address Register 1 (BAR 1)				14h
Base Address Register 2 (BAR 2)				18h
Base Address Register 3 (BAR 3)				1Ch
Base Address Register 4 (BAR 4)				20h
Base Address Register 5 (BAR 5)				24h
CardBus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capabilities Pointer	34h
Reserved				38h
Max Latency	Min Grant	Interrupt Pin	Interrupt Line	3Ch

The PCE243 OPT can be identified on the PCI bus during enumeration by the following PCI configuration registers:

Register	Power-On Value
Vendor ID	9030h
Device ID	10B5h
Revision	0293h
Class Code	0680h
Subsystem ID	9030h
Subsystem Vendor ID	10B5h

Note: The Vendor ID is the PLX vendor ID and may cause driver conflicts with operating systems such as Windows where existing drivers based on the Vendor and Device IDs pre-exist. If needed, these identifiers can be changed by modifying the contents of the serial EEPROM.

Most operating systems provide functions for finding devices on the PCI bus. These functions typically key off the Vendor and Device IDs, or the Class Code. Because the Class Code for the PCE243 OPT appears as a PCI Bridge with sub class code "other", it is recommended to key the search off the Vendor and Device IDs.

4.2 PCE243 OPT Configuration

The PCE243 OPT has two memory mapped register spaces and one I/O mapped register space. The address locations of the various spaces are determined by the Base Address Registers of the PCI configuration registers. Base Address Register 0 (BAR0) of the PCI configuration registers contains the address of the memory mapped PLX configuration registers. BAR1 contains the I/O address for the same PLX configuration registers. The PLX configuration registers are mapped into both memory and I/O space, so that these registers can be accessed via memory accesses or I/O addressing. BAR3 contains the address of the memory mapped OTG243 registers. Figure 4-1 illustrates the register mappings within a PCI system.

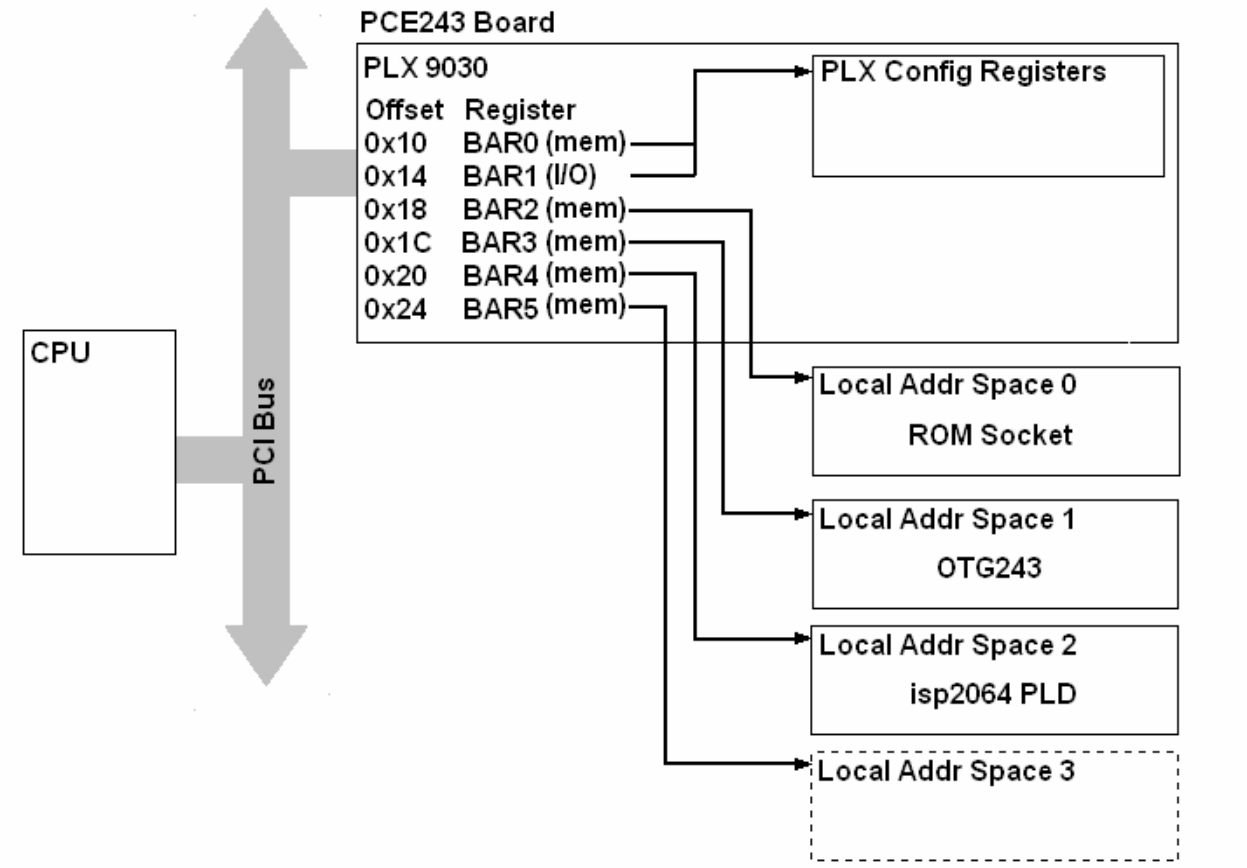


Figure 4-1. PCE243 OPT Register Mappings.

The Base Address Registers are typically initialized by the system BIOS, or by the operating system. Software generally does not have to manually set the addresses of the mapped locations, however, this is system dependent. If these registers are not initialized, the five address spaces

should be manually mapped into system memory and I/O space accordingly. Care must be taken to insure no conflicts exist between the mapped regions and other devices on the PCI bus.

4.3 PLX Configuration Registers

The Serial EEPROM contains hard coded configuration information for the PLX part and upon power up, the PLX chip reads the Serial EEPROM and loads the information into its configuration registers. Section 6.0 describes the serial EEPROM defaults. The PLX 9030 datasheet should be referenced for additional information. This section highlights the address decoding of the various chip selects from PCI address space to the PLX local address space.

There are four main registers that require configuration for each chip select. In addition, the I/O register must also be configured to setup the PLX pins to operate as chip selects rather than general purpose I/O. The main registers requiring configuration are as follows:

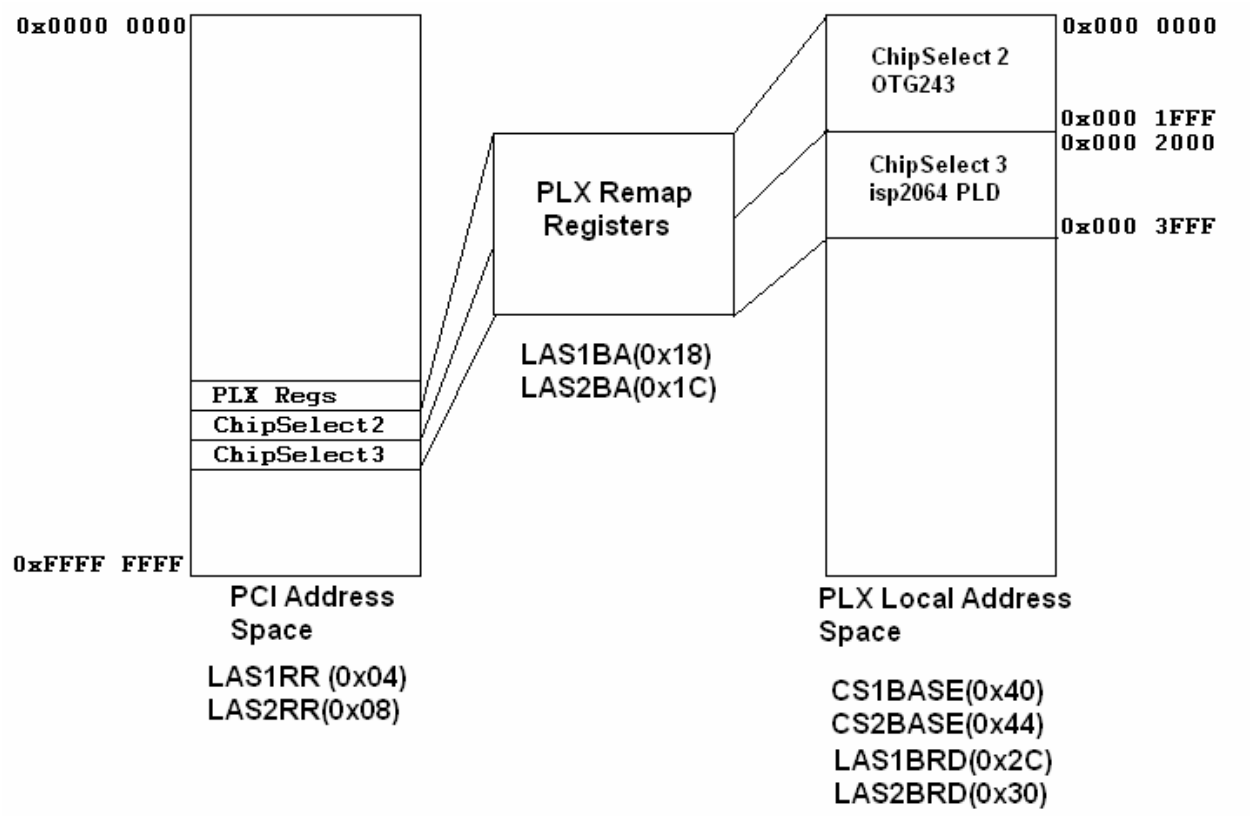


Figure 4-2 PCI and PLX Local Bus Address Mapping.

Figure 4-2 illustrates the mapping between PCI and PLX local address space. The addresses assigned in the PCI configuration registers for BAR3 and BAR4 are used as the base addresses for accessing the OTG243 and isp2064 respectively. There are four main registers that require configuration for each chip select. In addition, the general purpose I/O control must also be configured such that the general purpose I/O pins are used as chip selects.

To address the OTG243, use the value in BAR3 as the base address to the OTG243, which is accessed 32 bits at a time. To address the isp2064, use the value of BAR4 as the base address of the isp2064, which is accessed 8 bits at a time.

5.0 isp2064 Register Interface

Interrupt Event Register – (0x00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D+ High	D+ Low	D-High	D- Low	Vbus 0 - 0.6V	Vbus 0.6 – 1.5V	Vbus 1.5-4.4V	Vbus 4.4-5.0V

D+High	An interrupt will be generated when D+ is detected high.
D+Low	An interrupt will be generated when D+ is detected low
D-High	An interrupt will be generated when D- is detected high
D-Low	An interrupt will be generated when D- is detected low
Vbus 0-0.6V	An interrupt will be generated when Vbus is detected to be within the range of 0 to 0.6 volts.
Vbus 0.6-1.5V	An interrupt will be generated when Vbus is detected to be within the range of 0.6 to 1.5 volts.
Vbus 1.5-4.4V	An interrupt will be generated when Vbus is detected to be within the range of 1.5 to .4.4 volts.
Vbus 4.4-5V	An interrupt will be generated when Vbus is detected to be within the range of 4.4 to 5 volts.

This register is a read / write register. Writing a 1b to any bit in the register will set the bit, writing a 0b to any bit in the register will clear the bit. It is recommended that software perform a read-modify-write operation when handling the interrupt event register.

An interrupt will only be generated when a bit in the interrupt event register and its corresponding bit in the interrupt enable register are set.

Interrupt Enable Register – (0x04)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D+ High	D+ Low	D-High	D- Low	Vbus 0 - 0.6V	Vbus 0.6 – 1.5V	Vbus 1.5-4.4V	Vbus 4.4-5.0v

This register is a read / write register. Writing a 1b to any bit in the register will set the bit, writing a 0b to any bit in the register will clear the bit. It is recommended that software perform a read-modify-write operation when handling the interrupt mask.

An interrupt will only be generated when the enable bit is set for a particular interrupt.

USB Control Register – (0x08)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	SPD 2551	Suspend Enable	VBUS Control	VBUS PU Cntrl	ID Control	D- PU Control	D+ PU Control

D+ PU Control	Writing a one enables the VBUS PU Cntrl bit, writing a zero will disable VBUS PU Cntrl bit.
D- PU Control	Writing a one disables the D- Pull up, writing a zero will enable the D- Pull up.
VBUS PU Cntrl	If enabled by the D+ PU Control bit, writing a one drives the VBUS pull up, writing a zero drives the VBUS pull down.
VBUS Control	Writing a one turns on VBUS power, writing a zero disables VBUS power.
Suspend Enable	Writing a one suspends the Transceiver, writing a zero disables the suspend on the Transceiver.
SPD	Speed Control of Transceiver Writing a one indicates high speed. Writing a zero indicates low speed.
Reserved	Reserved

This register is a read / write register. Writing a 1b to any bit in the register will set the bit, writing a 0b to any bit in the register will clear the bit. It is recommended that software perform a read-modify-write operation when handling the control register.

USB Data Register – (0x0C)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
					TCVR Output Enable	VP	VM

VM	Read will provide the current state of VM A write will drive the VM signal to the transceiver causing VM to be driven when the output enable is set.
VP	Read will provide the current state of VP A write will drive the VP signal to the transceiver causing VP to be driven when the output enable is set.
TCVR Output Enable	Enables the transceiver to drive D+ and D- on the USB bus with the values in VM and VP. Writing a one enables the output from the transceiver. Writing a zero disables the output from the transceiver.

6.0 Serial EEPROM

6.1 Contents

The PLX 9030 provides an interface to program the attached serial EEPROM. The Serial EEPROM should be pre-programmed with the following default values. The table provided here is for informational purposes only. If the default values are modified, the behavior of the PCE243 OPT will change.

Serial EEPROM Offset	Description	Default
00h	PCI Device ID	9030h
02h	PCI Vendor ID	10B5h
04h	PCI Status Register	0290h
06h	PCI Command Register	Reserved
08h	PCI Class Code	0680h
0Ah	PCI Class Code / Revision Number	0001h
0Ch	PCI Subsystem ID	9030h
0Eh	PCI Subsystem Vendor ID	10B5h
10h	MSB New Capability Pointer	Reserved
12h	LSB New Capability Pointer	0040h
14h	(Maximum Latency and Minimum Grant are not loadable)	Reserved
16h	Interrupt Pin (Interrupt Line Routing is not loadable)	0100h
18h	MSW of Power Management Capabilities	0481h
1Ah	LSW of Power Management Next Capability Pointer / Power Management Capability ID	0481h
1Ch	MSW of Power Management Data /PMCSR Bridge Support Extension	Reserved
1Eh	LSW of Power Management Control/Status	0000h
20h	MSW of Hot Swap Control/Status	Reserved
22h	LSW of Hot Swap Next Capability Pointer / Hot Swap Control	4C06h
24h	PCI Vital Product Data Address	Reserved
26h	PCI Vital Product Data Next Capability Pointer / PCI Vital Protocol Data Control	0003h
28h	MSW of Local Address Space 0 Range	0000h
2Ah	LSW of Local Address Space 0 Range	0000h
2Ch	MSW of Local Address Space 1 Range	0FFFh
2Eh	LSW of Local Address Space 1 Range	E000h
30h	MSW of Local Address Space 2 Range	0FFFh
32h	LSW of Local Address Space 2 Range	E000h
34h	MSW of Local Address Space 3 Range	0000h
36h	LSW of Local Address Space 3 Range	0000h
38h	MSW of Expansion ROM Range	0000h

3Ah	LSW of Expansion ROM Range	0000h
3Ch	MSW of Local Address Space 0 Local Base Address (Remap)	0000h
3Eh	LSW of Local Address Space 0 Local Base Address (Remap)	0000h

Serial EEPROM Offset	Description	Default
40h	MSW of Local Address Space 1 Local Base Address (Remap)	0000h
42h	LSW of Local Address Space 1 Local Base Address (Remap)	0001h
44h	MSW of Local Address Space 2 Local Base Address (Remap)	0000h
46h	LSW of Local Address Space 2 Local Base Address (Remap)	2001h
48h	MSW of Local Address Space 3 Local Base Address (Remap)	0000h
4Ah	LSW of Local Address Space 3 Local Base Address (Remap)	0000h
4Ch	MSW of Expansion ROM Local Base Address (Remap)	0010h
4Eh	LSW of Expansion ROM Local Base Address (Remap)	0000h
50h	MSW of Local Address Space 0 Bus Region Descriptor	0080h
52h	LSW of Local Address Space 0 Bus Region Descriptor	0000h
54h	MSW of Local Address Space 1 Bus Region Descriptor	4080h
56h	LSW of Local Address Space 1 Bus Region Descriptor	0000h
58h	MSW of Local Address Space 2 Bus Region Descriptor	4001h
5Ah	LSW of Local Address Space 2 Bus Region Descriptor	80C0h
5Ch	MSW of Local Address Space 3 Bus Region Descriptor	0080h
5Eh	LSW of Local Address Space 3 Bus Region Descriptor	0000h
60h	MSW of Expansion ROM Bus Region Descriptor	0000h
62h	LSW of Expansion ROM Bus Region Descriptor	0000h
64h	MSW of Chip Select 0 Base Address	0BFFh
66h	LSW of Chip Select 0 Base Address	FFC1h
68h	MSW of Chip Select 1 Base Address	0000h
6Ah	LSW of Chip Select 1 Base Address	1001h
6Ch	MSW of Chip Select 2 Base Address	0000h
6Eh	LSW of Chip Select 2 Base Address	3001h
70h	MSW of Chip Select 3 Base Address	0000h
72h	LSW of Chip Select 3 Base Address	0000h
74h	Serial EEPROM Write-Protected Address Boundary	0030h
76h	LSW of Interrupt Control/Status	0041h
78h	MSW of Target Response, Serial EEPROM, and initialization Control	0870h
7Ah	LSW of Target Response, Serial EEPROM, and initialization Control	0000h
7Ch	MSW of General Purpose I/O Control	0024h
7Eh	LSW of General Purpose I/O Control	9864h
80h	MSW of Hidden 1 Power Management Data Select	0000h
82h	LSW of Hidden 1 Power Management Data Select	0000h
84h	MSW of Hidden 2 Power Management Data Select	0000h

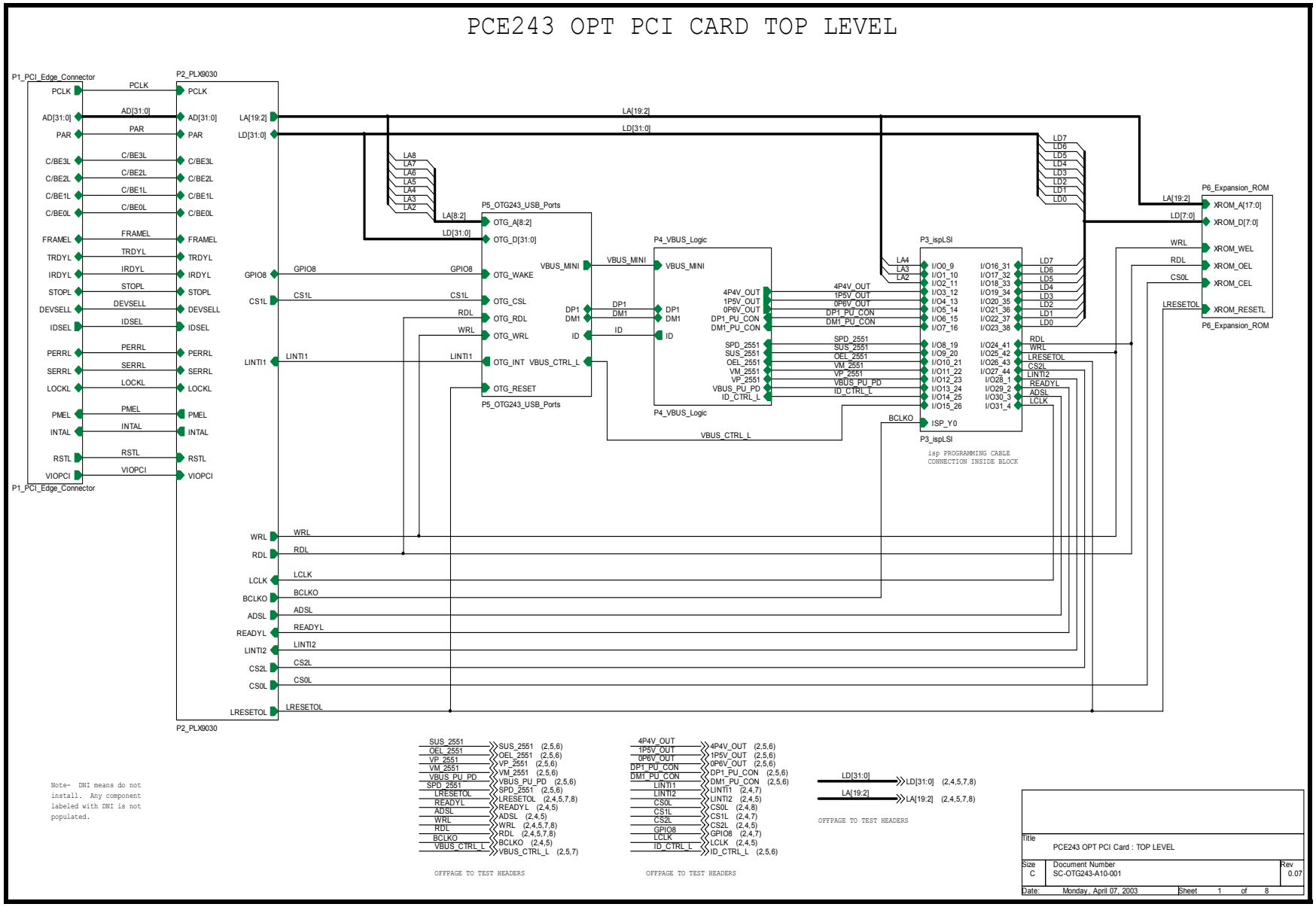
86h	LSW of Hidden 2 Power Management Data Select	0000h

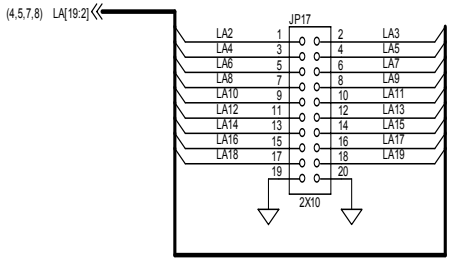
7.0 References

- USB 2.0 Specification (www.usb.org)
- USB On-The-Go Supplement to USB 2.0 Specification (www.usb.org)
- OTG243 Data Sheet (TDI Document Number: MU2001)

8.0 Schematics

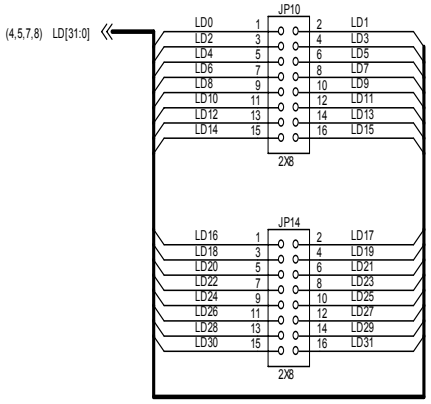
The schematics of the PCE243 OPT are presented in the next section of this document.


PCE243 OPT PCI CARD TOP LEVEL
P1_PCI_Edge_Connector
P2_PLX9030
P5_OTG243_USB_Ports
P4_VBUS_Logic
P3_ispLSI
P6_Expansion_ROM
isp PROGRAMMING CABLE CONNECTION INSIDE BLOCK
OFFPAGE TO TEST HEADERS
Note- DNI means do not install. Any component labeled with DNI is not populated.
Title
PCE243 OPT PCI Card : TOP LEVEL
Size C
Document Number SC-OTG243-A10-001
Rev 0.07
Date: Monday, April 07, 2003
Sheet 1 of 8



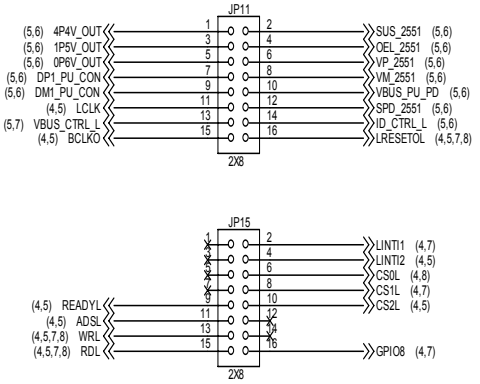
LOCAL ADDRESS BUS TEST HEADERS

SILKSCREEN HEADERS TO
IDENTIFY THE CONNECTIONS



LOCAL DATA BUS TEST HEADERS

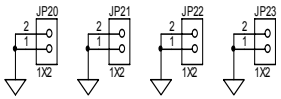
SILKSCREEN HEADERS TO
IDENTIFY THE CONNECTIONS



ISP TEST HEADERS

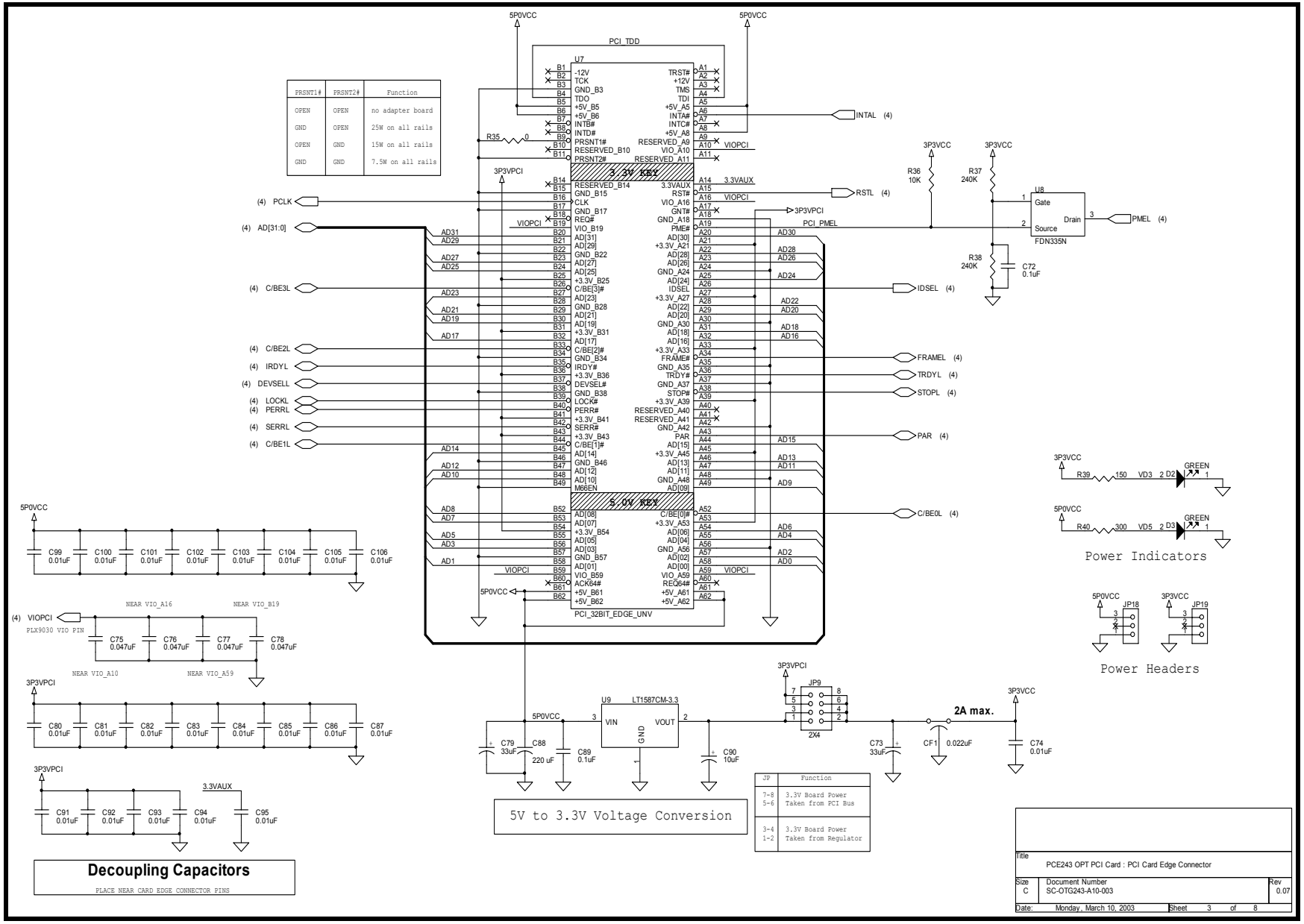
SILKSCREEN HEADERS TO
IDENTIFY THE CONNECTIONS

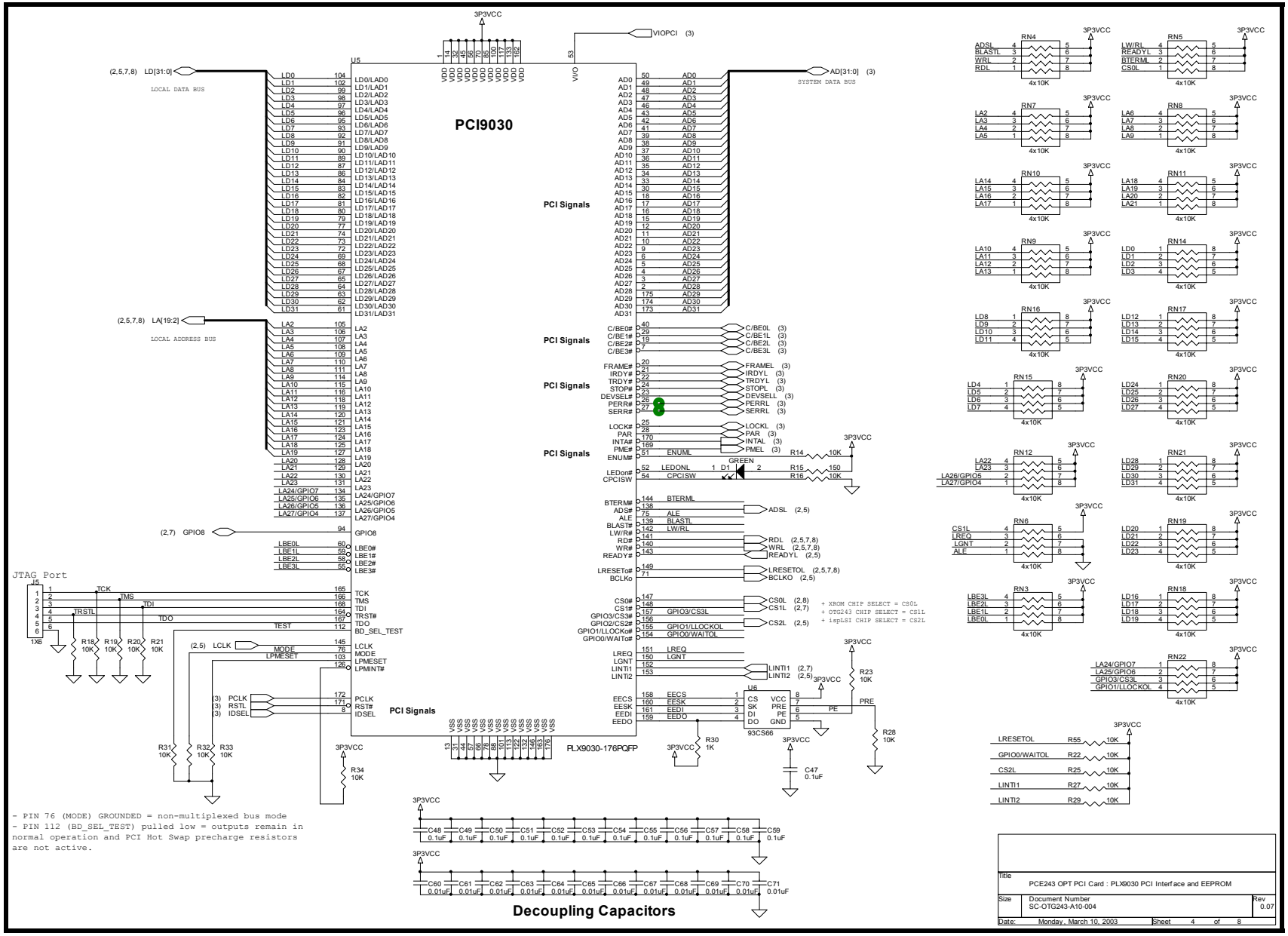
Distribute the TestPoints
near top side and corners

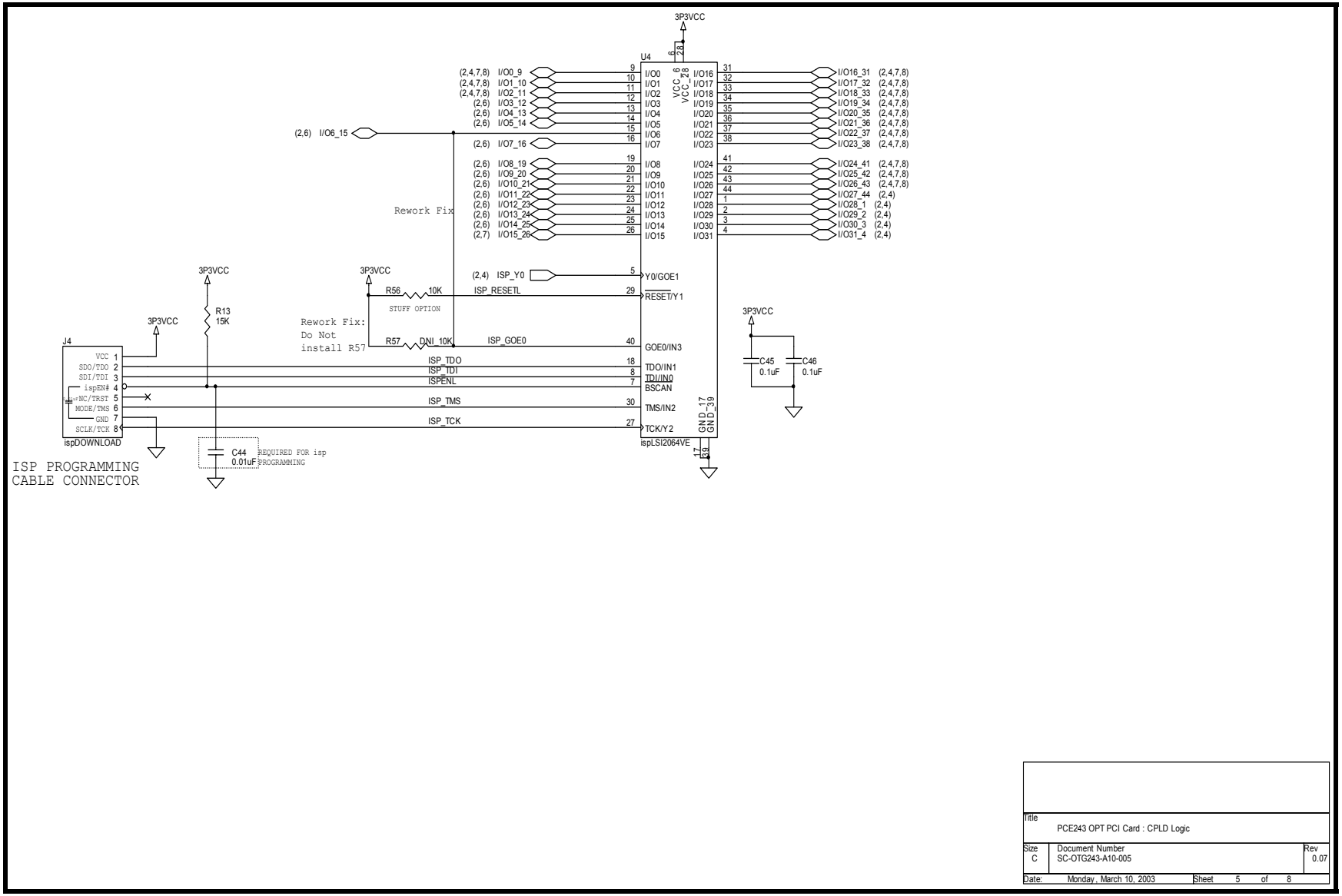


GROUND TEST POINTS

Title: PCE243 OPT PCI Card : Test Headers		
Size: C	Document Number: SC-OTG243-A10-002	Rev: 0.07
Date: Monday, April 07, 2003	Sheet 2 of 8	


PCI_TDD
U7
3.3V KEY
5.0V KEY
PCI_32BIT_EDGE_UNV
5P0VCC
3P3VPCI
3P3VCC
VIOPCI
3.3VAUX
PRSNT1# PRSNT2# Function
OPEN OPEN no adapter board
GND OPEN 25W on all rails
OPEN GND 15W on all rails
GND GND 7.5W on all rails
INTAL (4)
RSTL (4)
IDSEL (4)
FRAMEL (4)
TRDYL (4)
STOPL (4)
PAR (4)
C/BE0L (4)
PMEL (4)
PCI_PMEL
FDN335N
Power Indicators
Power Headers
Decoupling Capacitors
PLACE NEAR CARD EDGE CONNECTOR PINS
5V to 3.3V Voltage Conversion
2A max.
JP Function
7-8 5-6 3.3V Board Power Taken from PCI Bus
3-4 1-2 3.3V Board Power Taken from Regulator
Title PCE243 OPT PCI Card : PCI Card Edge Connector
Size C
Document Number SC-OTG243-A10-003
Rev 0.07
Date: Monday, March 10, 2003
Sheet 3 of 8


PCI9030
PLX9030-176PQFP
LOCAL DATA BUS
LOCAL ADDRESS BUS
SYSTEM DATA BUS
PCI Signals
JTAG Port
93CS66
Decoupling Capacitors
- PIN 76 (MODE) GROUNDED = non-multiplexed bus mode
- PIN 112 (BD_SEL_TEST) pulled low = outputs remain in normal operation and PCI Hot Swap precharge resistors are not active.
+ XROM CHIP SELECT = CS0L
+ OTG243 CHIP SELECT = CS1L
+ ispLSI CHIP SELECT = CS2L
PCE243 OPT PCI Card : PLX9030 PCI Interface and EEPROM
Document Number SC-OTG243-A10-004
Monday, March 10, 2003


3P3VCC
U4
VCC_6
VCC_28
(2,4,7,8) I/O0_9
(2,4,7,8) I/O1_10
(2,4,7,8) I/O2_11
(2,6) I/O3_12
(2,6) I/O4_13
(2,6) I/O5_14
(2,6) I/O6_15
(2,6) I/O7_16
(2,6) I/O8_19
(2,6) I/O9_20
(2,6) I/O10_21
(2,6) I/O11_22
(2,6) I/O12_23
(2,6) I/O13_24
(2,6) I/O14_25
(2,7) I/O15_26
I/O16_31 (2,4,7,8)
I/O17_32 (2,4,7,8)
I/O18_33 (2,4,7,8)
I/O19_34 (2,4,7,8)
I/O20_35 (2,4,7,8)
I/O21_36 (2,4,7,8)
I/O22_37 (2,4,7,8)
I/O23_38 (2,4,7,8)
I/O24_41 (2,4,7,8)
I/O25_42 (2,4,7,8)
I/O26_43 (2,4,7,8)
I/O27_44 (2,4)
I/O28_1 (2,4)
I/O29_2 (2,4)
I/O30_3 (2,4)
I/O31_4 (2,4)
Rework Fix
(2,4) ISP_Y0
R56 10K
ISP_RESETL
STUFF OPTION
Rework Fix:
Do Not
install R57
R57 DNI_10K
ISP_GOE0
Y0/GOE1
RESET/Y1
GOE0/IN3
TDO/IN1
TDI/IN0
BSCAN
TMS/IN2
TCK/Y2
ispLSI2064VE
GND_17
GND_39
R13
15K
J4
VCC 1
SDO/TDO 2
SDI/TDI 3
ispEN# 4
NC/TRST 5
MODE/TMS 6
GND 7
SCLK/TCK 8
ispDOWNLOAD
ISP_TDO
ISP_TDI
ISPENL
ISP_TMS
ISP_TCK
C44
0.01uF
REQUIRED FOR isp
PROGRAMMING
C45
0.1uF
C46
0.1uF
ISP PROGRAMMING
CABLE CONNECTOR
Title
PCE243 OPT PCI Card : CPLD Logic
Size C
Document Number SC-OTG243-A10-005
Rev 0.07
Date: Monday , March 10, 2003
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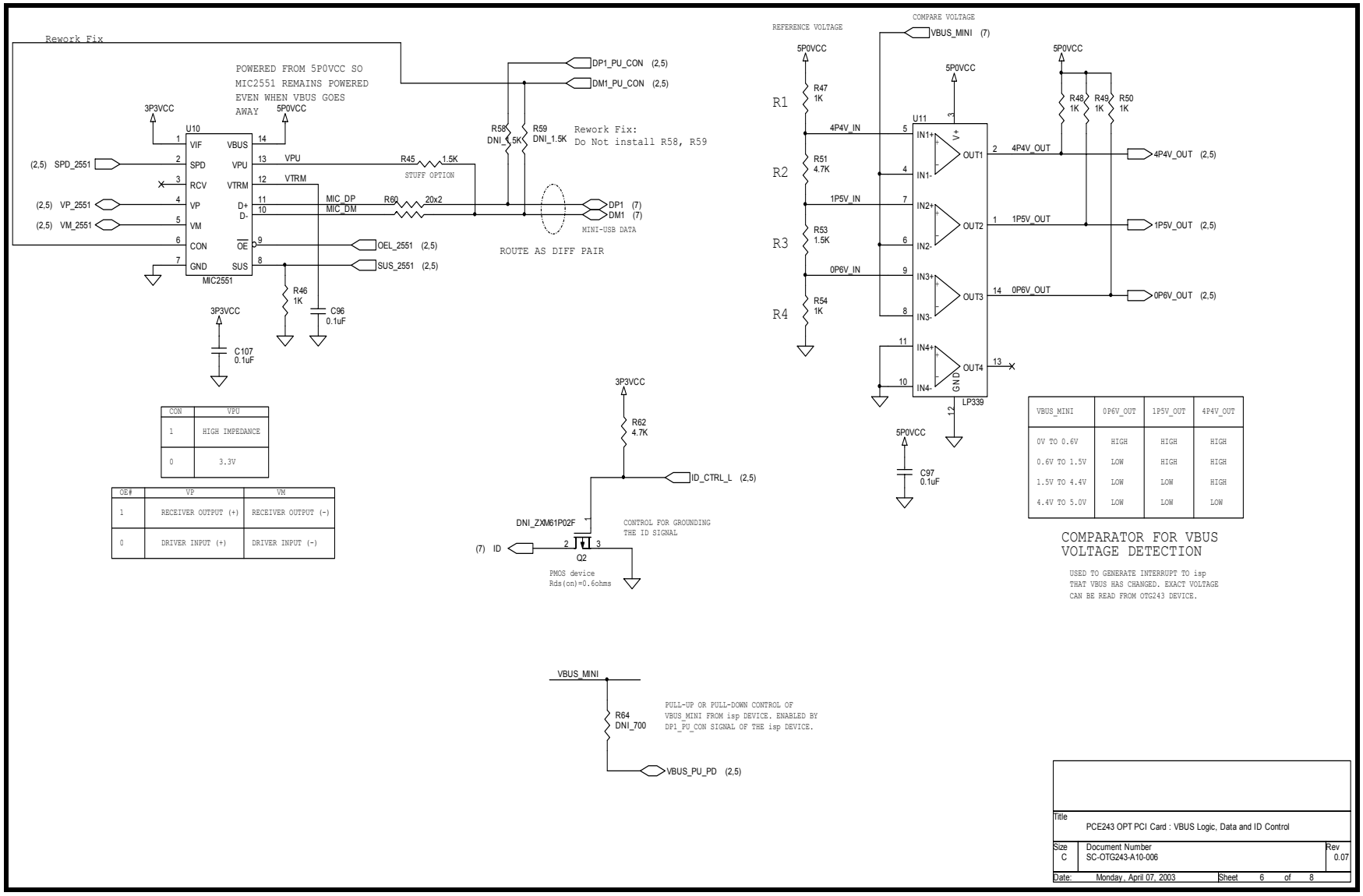
Rework Fix
POWERED FROM 5P0VCC SO MIC2551 REMAINS POWERED EVEN WHEN VBUS GOES AWAY
3P3VCC
5P0VCC
U10
VIF
VBUS
SPD
VPU
RCV
VTRM
VP
D+
VM
D-
CON
OE
GND
SUS
MIC2551
(2,5) SPD_2551
(2,5) VP_2551
(2,5) VM_2551
VPU
VTRM
MIC_DP
MIC_DM
R45 1.5K
STUFF OPTION
R60 20x2
R58 DNI_1.5K
R59 DNI_1.5K
Rework Fix:
Do Not install R58, R59
DP1_PU_CON (2,5)
DM1_PU_CON (2,5)
DP1 (7)
DM1 (7)
MINI-USB DATA
ROUTE AS DIFF PAIR
OEL_2551 (2,5)
SUS_2551 (2,5)
R46 1K
C96 0.1uF
C107 0.1uF
CON
VPU
1
HIGH IMPEDANCE
0
3.3V
OE#
VP
VM
1
RECEIVER OUTPUT (+)
RECEIVER OUTPUT (-)
0
DRIVER INPUT (+)
DRIVER INPUT (-)
3P3VCC
R62 4.7K
ID_CTRL_L (2,5)
DNI_ZXM61P02F
CONTROL FOR GROUNDING THE ID SIGNAL
(7) ID
Q2
PMOS device
Rds(on)=0.6ohms
REFERENCE VOLTAGE
COMPARE VOLTAGE
VBUS_MINI (7)
5P0VCC
R1
R2
R3
R4
R47 1K
R51 4.7K
R53 1.5K
R54 1K
4P4V_IN
1P5V_IN
0P6V_IN
U11
IN1+
IN1-
IN2+
IN2-
IN3+
IN3-
IN4+
IN4-
OUT1
OUT2
OUT3
OUT4
V+
GND
LP339
4P4V_OUT
1P5V_OUT
0P6V_OUT
R48 1K
R49 1K
R50 1K
4P4V_OUT (2,5)
1P5V_OUT (2,5)
0P6V_OUT (2,5)
C97 0.1uF
VBUS_MINI
0P6V_OUT
1P5V_OUT
4P4V_OUT
0V TO 0.6V
HIGH
HIGH
HIGH
0.6V TO 1.5V
LOW
HIGH
HIGH
1.5V TO 4.4V
LOW
LOW
HIGH
4.4V TO 5.0V
LOW
LOW
LOW
COMPARATOR FOR VBUS VOLTAGE DETECTION
USED TO GENERATE INTERRUPT TO isp THAT VBUS HAS CHANGED. EXACT VOLTAGE CAN BE READ FROM OTG243 DEVICE.
VBUS_MINI
R64 DNI_700
PULL-UP OR PULL-DOWN CONTROL OF VBUS_MINI FROM isp DEVICE. ENABLED BY DP1_PU_CON SIGNAL OF THE isp DEVICE.
VBUS_PU_PD (2,5)
Title
PCE243 OPT PCI Card : VBUS Logic, Data and ID Control
Size C
Document Number SC-OTG243-A10-006
Rev 0.07
Date: Monday, April 07, 2003
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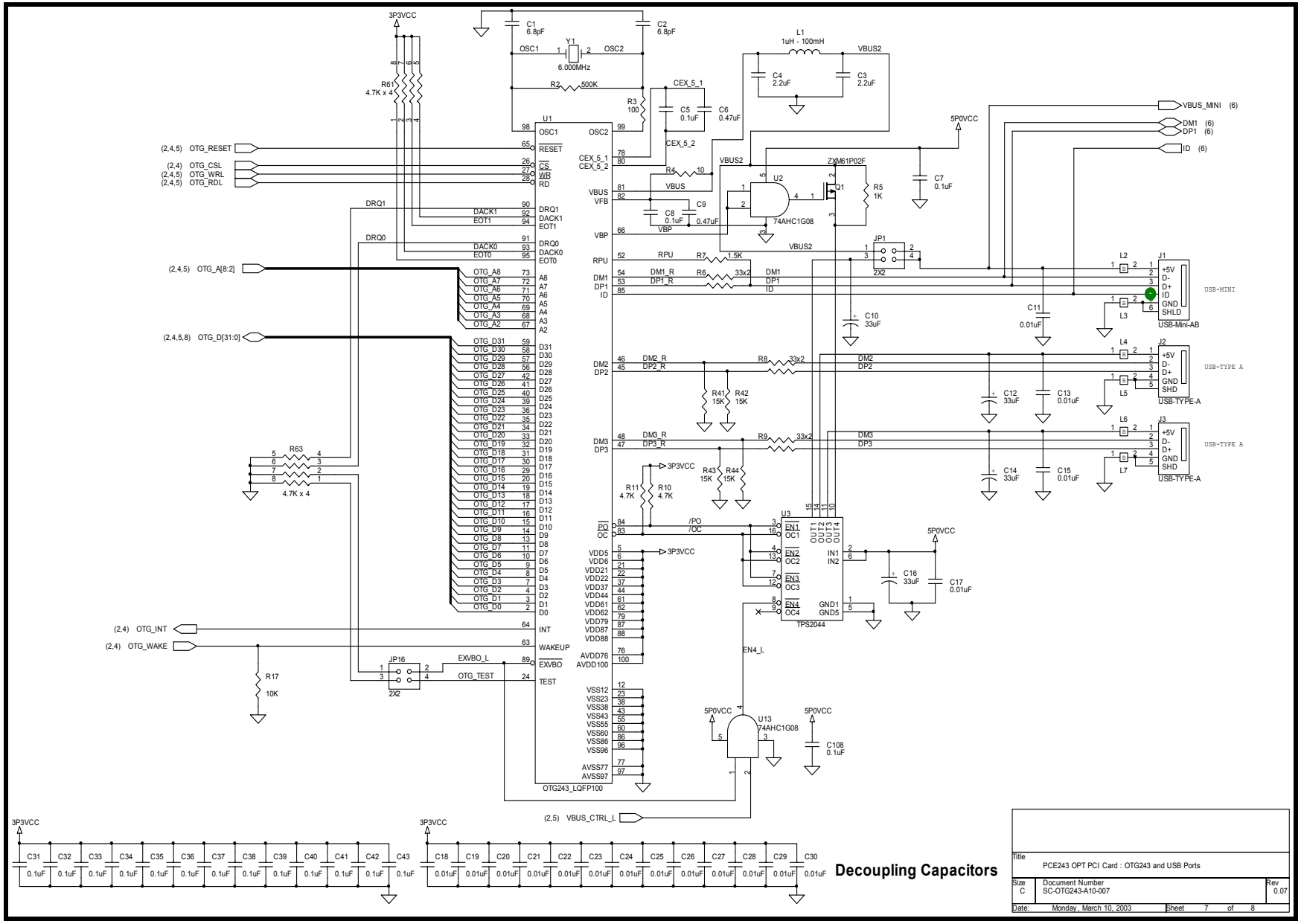
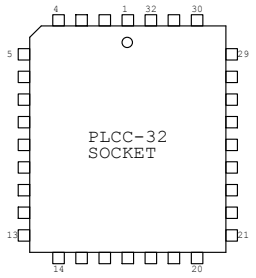
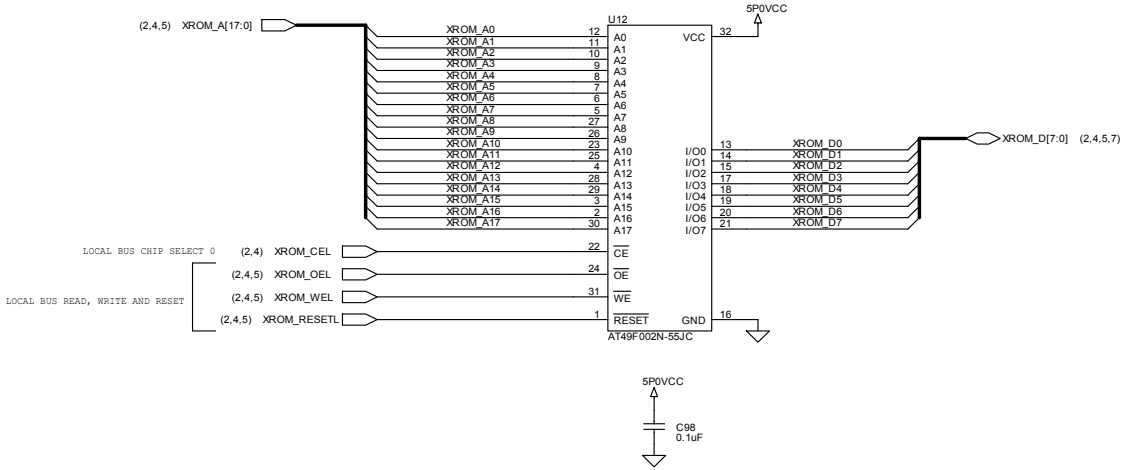

Decoupling Capacitors
PCE243 OPT PCI Card : OTG243 and USB Ports
SC-OTG243-A10-007
Monday, March 10, 2003
OTG243_LQFP100
TPS2044
74AHC1G08
USB-MINI
USB-Mini-AB
USB-TYPE A
USB-TYPE-A





Title	PCE243 OPT PCI Card : PCI Expansion Boot FLASH ROM	
Size C	Document Number SC-OTG243-A10-008	Rev 0.07
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